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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,216	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending.

2. The office acknowledges the following papers:

Specification, claims, arguments, and drawings filed on 11/7/2006.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation from claim 10 "the determining independent of the form of the instruction" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

New Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 10-14 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 10 recites the limitation "the determining independent of the form of the instruction." In paragraphs 17-18 of the specification, regular java bytecodes and complex bytecodes are described. A simple bytecode is an instruction that can execute in a single or several cycles. A complex bytecode takes longer and may be replaced by a micro-sequence of other instructions. Paragraph 26 of the specification describes using a micro-sequence vector table to store all of the bytecodes and use a bit to determine if the bytecode will be replaced by a micro-sequence. A form of the instruction is interpreted as including parts of the instruction that identify what and how the instruction is to operation. When initially loading the micro-sequence vector table, the form of the instruction must be taken into consideration when determining which bytecodes will be replaced by a micro-sequence and what the address will be to point to this sequence of instructions. The specification doesn't enable one of ordinary skill in the art as to how determining which bytecodes will be replaced doesn't take into consideration the form of the instruction without causing undue burden and/or experimentation. For examination purposes, the additional limitation will not be considered.

6. Claims 10-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 10 recites the limitation "the determining independent of the form of the instruction." In paragraphs 17-18 of the specification, regular java bytecodes and complex bytecodes are described. A simple bytecode is an instruction that can execute in a single or several cycles. A complex bytecode takes longer and may be replaced by a micro-sequence of other instructions. Paragraph 26 of the specification describes using a micro-sequence vector table to store all of the bytecodes and use a bit to determine if the bytecode will be replaced by a micro-sequence. A form of the instruction is interpreted as including parts of the instruction that identify what and how the instruction is to operation. When initially loading the micro-sequence vector table, the form of the instruction must be taken into consideration when determining which bytecodes will be replaced by a micro-sequence and what the address will be to point to this sequence of instructions. Thus, there isn't any support within the specification at the time the application was filed to support the additional limitation.

7. Claims 11-14 are rejected due to their dependency.

Maintained Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United

States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claims 10 and 13 are rejected under 35 U.S.C. §102(e) as being anticipated by Gee (U.S. 6,317,872).

10. As per claim 10:

Gee disclosed a method comprising:

Fetching an instruction (Gee: Figure 1 element 104, column 8 lines 63-67)(The instructions are fetched from element 104); and

Determining whether said instruction is to be executed or replaced by a group of other instructions (Gee: Figure 2 element 200, column 9 lines 5-52)(The control store contains the micro sequence for each macro java bytecode and is used to replace the bytecode.).

11. As per claim 13:

Gee disclosed the method of claim 10 further including switching an active program counter between two program counters when replacing the instruction with the group of instructions (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is selected to fetch and execute the micro program. Thus having the same functionality.).

New Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 10-12, 14, and 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Zaidi (U.S. 6,581,154).

14. As per claim 10:

Zaidi disclosed a method comprising:

Fetching an instruction (Zaidi: Figure 2 element 205, column 3 lines 55-67 continued to column 4 lines 1-7)(Instructions are fetched by macroinstructions from the uROM.); and

Determining whether said instruction is to be executed or replaced by a group of other instructions (Zaidi: Figure 2 elements 203, 205, and 210, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer translates macroinstructions into Uops and Suops. The instructions stored in the uROM are executed or replaced depending on if they are Uops or Suops. It's obvious to one of ordinary skill in the art that after the instructions are fetched from the uROM, there must be a determining step that determines if the instruction fetched is a Uop that needs to be sent directly to be executed or if the instruction fetched is a Suop that needs to be replaced by a other instructions in the expander element.).

15. As per claim 11:

Zaidi disclosed the method of claim 10 further including replacing the instruction with said group of other instructions (Zaidi: Figure 2 element 210, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer logic determines if the

instruction is a Uop or a Suop that will further be expanded and replaced by a group of instructions.).

16. As per claim 12:

Zaidi disclosed the method of claim 10 wherein determining whether the instruction is to be executed or replaced includes determining a value of a bit associated with the instruction (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both Uops and Suops. The S U ops are to be further expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The Uops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

17. As per claim 14:

Zaidi disclosed the method of claim 10 further including programming a table to specify which instructions are to be executed directly and which instructions are to be replaced by a group of instructions (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both Uops and Suops. The Suops are to be further expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The Uops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

18. As per claim 22:

Zaidi disclosed a processor, comprising:

Decode logic that decodes instructions (Zaidi: Figure 1 element 110, column 3 lines 34-39); and

A means for determining whether an instruction is to be executed or replaced by a micro-sequence of other instructions (Zaidi: Figure 2 elements 203, 205, and 210, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer translates macroinstructions into Uops and Suops. The instructions stored in the uROM are executed or replaced depending on if they are Uops or Suops. It's obvious to one of ordinary skill in the art that after the instructions are fetched from the uROM, there must be a determining step that determines if the instruction fetched is a Uop that needs to be sent directly to be executed or if the instruction fetched is a Suop that needs to be replaced by a other instructions in the expander element.).

19. As per claim 23:

Zaidi disclosed the processor of claim 22 further including a means for replacing the instruction with the micro-sequence (Zaidi: Figure 2 element 203, column 3 lines 55-67 continued to column 4 lines 1-7)(The micro instruction sequencer logic determines if the instruction is a Uop or a S Uop that will further be expanded and replaced by a group of instructions.).

20. Claims 18 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Seal et al. (U.S. 6,965,984).

21. As per claim 18:

Seal disclosed an electronic device, comprising:

Decode logic that decodes instructions, the decode logic decodes instructions from a first instruction set and a second instruction set, the second instruction set different from the first instruction set (Seal: Figure 1 element 6, column 5 lines 60-67 continued to column 6 lines 1-9)(It's obvious to one of ordinary skill in the art at the time of the invention that there would have to be some sort of predecoding done to initially detect java bytecodes to send to element 6 or detect ARM opcodes that will be bypassed around element 6. The first and second instruction sets are the java bytecodes and the ARM opcodes, which are different from each other.); and

A vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a first field indicating whether the corresponding instruction is to be executed by the electronic device or whether the instruction is to be replaced by a predetermined group of instructions stored in memory (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality.).

22. As per claim 21:

Seal disclosed the electronic device of claim 18 wherein the group of instructions terminates with a predetermined instruction (Seal: Figure 2 element 26, column 7 lines 24-40)(The BXJ instruction will cause a group of instructions to terminate. Thus having the same functionality.).

23. Claims 1-4, 7-9, and 19-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Seal et al. (U.S. 6,965,984), in view of Gee et al. (U.S. 6,317,872).

24. As per claim 1:

Seal disclosed a processor comprising:

Fetch logic that retrieves instructions from memory (It's obvious to one of ordinary skill in the art that fetch logic exists to fetch the Java bytecodes and ARM bytecodes.);

Decode logic coupled to said fetch logic, the decode logic decodes instructions from a first instruction set and a second instruction set, the second instruction set different than the first instruction set (Seal: Figure 1 element 6, column 5 lines 60-67 continued to column 6 lines 1-9)(It's obvious to one of ordinary skill in the art at the time of the invention that there would have to be some sort of predecoding done to initially detect java bytecodes to send to element 6 or detect ARM opcodes that will be bypassed around element 6. The first and second instruction sets are the java bytecodes and the ARM opcodes, which are different from each other.);

Wherein an instruction of the first instruction set is replaced by a micro-sequence comprising one or more instructions of the second instruction set (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality. The first instruction set is the Java bytecodes and the second is the ARM opcodes.).

Seal failed to teach an active program counter selected as either a first program

counter or a second program counter and the active program counter switches between the first and second program counters.

However, Gee disclosed an active program counter selected as either a first program counter or a second program counter (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is selected to fetch and execute the micro program. Thus having the same functionality. When combined with Seal, the primary program counter would also work with the ARM opcodes that are normally fetched. The micro program counter would be used with the plurality of ARM opcodes that a single Java bytecode is translated into.); and

The active program counter switches between the first and second program counters (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is used to fetch and execute the micro program. Thus having the same functionality.).

Seal disclosed a method of translating a single java bytecode into a plurality of ARM opcodes through using a table and address pointers. Seal failed to teach how to differentiate the microinstructions from one another when they are executed because they all will share the same program counter from the initial fetched java bytecode. One of ordinary skill in the art would have been motivated by this to find Gee using a micro-program counter for microcode instructions generated from macroinstructions. Thus, it

would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two program counters for the advantage of allowing for translated java bytecodes into a plurality of ARM opcodes to be tracked through the processor.

25. As per claim 2:

Seal and Gee disclosed the processor of claim 1, including a vector table accessible by said decode logic, said vector table including information which specifies whether an instruction is to be replaced by a micro-sequence (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality.).

26. As per claim 3:

Seal and Gee disclosed the processor of claim 2 wherein the information is provided to the vector table from a block of memory accessible to the processor by an indirect addressing mode used in a repeat loop comprising at least one instruction (Seal: Figure 10, column 10 lines 34-67 continued to column 11 lines 1-20)(The vector table is initialized with value in a repeat loop shown in figure 10.).

27. As per claim 4:

Seal and Gee disclosed the processor of claim 2 wherein the vector table comprises a plurality of entries and any one entry can be modified independently of the other entries (Seal: Figure 10 element 120, column 10 lines 34-67 continued to column 11 lines 1-20)(Upon initialization, each entry is written independently of each other. Thus having the same functionality.).

28. As per claim 7:

Seal and Gee disclosed the processor of claim 1 wherein the active program counter again switches between the first and second program counters when the micro-sequence is completed (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(Upon the completion of the micro program, another macro java bytecode is fetched to execute. With the micro PC not fetching and executing the micro program, the PC will fetch additional java bytecodes as the active PC.).

29. As per claim 8:

Seal and Gee disclosed the processor of claim 1 wherein the second program counter is used to fetch and decode instructions comprising a micro-sequence and switching between the first and second program counters comprises switching from the first program counter to the second program counter and loading the second program counter with a starting address of the micro-sequence (Gee: Figure 2 elements 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(Figure two shows that the micro PC is used to index into the micro instruction storage to fetch instructions. It's inherent then that the micro PC is given the starting address of the micro sequence of instructions to correctly fetch and execute them.).

30. As per claim 9:

Seal and Gee disclosed the processor of claim 1 wherein a plurality of instructions are replaceable by a corresponding micro-sequence (Gee: Column 8 lines

50-62)(The macro java bytecodes are replaced by a pointer that points to a sequence of micro instructions.).

31. As per claim 19:

Seal disclosed the electronic device of claim 18.

Seal failed to teach further including an active program counter selected as either a first program counter or a second program counter, wherein an instruction is replaced by the group of instructions and the active program counter concurrently switches from the first to the second program counter.

However, Gee disclosed further including an active program counter selected as either a first program counter or a second program counter, wherein an instruction is replaced by the group of instructions and the active program counter concurrently switches from the first to the second program counter (Gee: Figure 2 element 204 and 226, column 8 lines 49-67 continued to column 9 lines 1-52)(The primary program counter, element 204, is functioning to fetch java bytecodes and the micro program counter, element 226, is selected to fetch and execute the micro program. Thus having the same functionality. The combination of Seal and Gee results in the micro program counter being used for when a plurality of ARM opcodes are generated for a single java bytecode.).

Seal disclosed a method of translating a single java bytecode into a plurality of ARM opcodes through using a table and address pointers. Seal failed to teach how to differentiate the micro-instructions from one another when they are executed because they all will share the same program counter from the initial fetched java bytecode. One

of ordinary skill in the art would have been motivated by this to find Gee using a micro-program counter for microcode instructions generated from macroinstructions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two program counters for the advantage of allowing for translated java bytecodes into a plurality of ARM opcodes to be tracked through the processor.

32. As per claim 20:

Seal disclosed the electronic device of claim 18.

Seal failed to teach wherein upon switching the active program counter, the first program counter is incremented.

However, Gee disclosed wherein upon switching the active program counter, the first program counter is incremented (Gee: Figure 2 elements 204 and 236, column 8 lines 49-67 continued to column 9 lines 1-52)(When another macro instruction is to be fetched from memory, the PC is incremented to insure that the correct instruction is fetched instead of an instruction previously fetched. Thus having the same functionality.).

Seal disclosed a method of translating a single java bytecode into a plurality of ARM opcodes through using a table and address pointers. Seal failed to teach how to differentiate the micro-instructions from one another when they are executed because they all will share the same program counter from the initial fetched java bytecode. One of ordinary skill in the art would have been motivated by this to find Gee using a micro-program counter for microcode instructions generated from macroinstructions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to

implement the two program counters for the advantage of allowing for translated java bytecodes into a plurality of ARM opcodes to be tracked through the processor.

33. Claims 5-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Seal et al. (U.S. 6,965,984), in view of Gee et al. (U.S. 6,317,872), further in view of Zaidi (U.S. 6,581,154).

34. As per claim 5:

Seal and Gee disclosed the processor of claim 1.

Seal and Gee failed to teach including a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and associated with a bit indicating whether the corresponding instruction is to be executed by the processor or whether the instruction is to be replaced by a micro-sequence.

However, Zaidi disclosed including a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and associated with a bit indicating whether the corresponding instruction is to be executed by the processor or whether the instruction is to be replaced by a micro-sequence (Zaidi: Figure 2 element 205, column 4 lines 1-7)(Element 205 stores both U ops and S U ops. The S U ops are to be further expanded and the bits associated with them indicate that they are to be replaced by a group of instruction by element 210. The U ops have bits associated with them that indicate no further expansion is needed and that they can be sent directly to the dispatch queue. Thus having the same functionality.).

Gee disclosed a processor that replaces macro java bytecodes with a micro

sequence of instructions. Gee disclosed that a java bytecode is essentially a pointer to a sequence of microinstructions (Gee: Column 8 lines 57-59). However, Gee doesn't disclose the process of the replacement. One of ordinary skill in the art would have been motivated by the lack of the disclosure on the replacement process to find additional details on the process. Zaidi disclosed using a vector table of entries that will replace a macroinstruction with microinstructions. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a vector table to contain pointers to the microinstructions that will replace the java bytecodes.

35. As per claim 6:

Seal, Gee, and Zaidi disclosed the processor of claim 5 wherein at least some of the entries include a reference to a memory location in which a micro-sequence is stored depending if the associated bit indicates that the instruction is to be replaced by a micro-sequence (Zaidi: Figure 2 elements 205 and 210, column 4 lines 1-7)(Element 205 inherently includes information about a memory location that stores the instructions to be replaced.).

36. Claim 15-17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Seal et al. (U.S. 6,965,984), in view of Gee et al. (U.S. 6,317,872), and in view of Greenberger et al. (U.S. 6,092,179).

37. As per claim 15:

Claim 15 essentially recites the same limitations of claim 1. Claim 15 additionally recites the following limitations:

Seal and Gee additionally disclosed a second processor (Gee: Figure 1 element 100).

Seal and Gee failed to teach a first processor coupled to the second.

However, Greenberger disclosed a first processor coupled to the second (Greenberger: Figure 2 elements 2 and 7, column 3 lines 49-67).

One technique to add new functionality to a processor is to add a co-processor with the added technique (Greenberger: Column 2 lines 1-20). One of ordinary skill in the art would have been motivated to add the combine the processor of Greenberger and Gee for the added functionality of executing macro java bytecodes and replacing them with a micro sequence. Thus, it would have been obvious to one of ordinary skill in the art to combine the two processors for the added functionality of executing java bytecodes.

38. As per claim 16:

Seal, Gee, and Greenberger disclosed the system of claim 15, wherein said second processor further includes a micro-sequence vector table comprising a plurality of entries, each entry corresponding to a separate instruction and including a field that indicates whether the corresponding instruction is to be executed by the second processor or whether the instruction is to be replaced by a micro-sequence (Seal: Figure 2 element 24, column 6 lines 60-67 continued to column 7 lines 1-23)(All of the entries in element 24 store pointers to a group of instructions that will replace the instruction. Thus having the same functionality.).

39. As per claim 17:

Claim 17 essentially recites the same limitations of claim 6. Therefore, claim 17 is rejected for the same reasons as claim 6.

Response to Arguments

40. The arguments presented by Applicant in the response, received on 11/7/2006 are not considered persuasive.

41. Applicant argues that "Seal failed to teach decode logic that decodes instructions, the decode logic decodes instructions from a first instruction set and a second instruction set, the second instruction set different from the first instruction set" for claims 1, 15, and 18.

This argument is not found to be persuasive for the following reason. While the examiner agrees that decoder element 10 no longer reads upon the claimed limitation, the examiner disagrees that Seal no longer reads upon the limitation. It's obvious to one of ordinary skill in the art at the time of the invention that there would have to be some sort of predecoding done to initially detect java bytecodes to send to element 6 or detect ARM opcodes that will be bypassed around element 6. The first and second instruction sets are the java bytecodes and the ARM opcodes, which are different from each other.

43. Applicant argues that "Gee fails to teach determining whether said instruction is to be executed or replace by a group of other instructions" for claim 10.

This argument is not found to be persuasive for the following reason. It's inherent that there is a determining step since each bytecode will be chosen to be replaced by a group of other instructions.

44. Applicant argues that "Zaidi fails to teach the determining independent of the form of the instruction" for claim 10.

This argument is not found to be persuasive for the following reason. This limitation hasn't been considered for examination purposes due to the enablement and written description rejections.

45. Applicant argues that "Zaidi fails to teach determining whether said instruction is to be executed or replace by a group of other instructions" for claims 10 and 22.

This argument is not found to be persuasive for the following reason. Applicant states that the macroinstruction is not executed since it's replaced with a Uop. The examiner agrees that the original macroinstruction is not executed, but disagrees that Zaidi no longer reads upon the claimed limitation. The microinstruction sequencer translates macroinstructions into Uops and Suops. The instructions stored in the uROM are executed or replaced depending on if they are Uops or Suops. It's obvious to one of ordinary skill in the art that after the instructions are fetched from the uROM, there must be a determining step that determines if the instruction fetched is a Uop that needs to be sent directly to be executed or if the instruction fetched is a Suop that needs to be replaced by a other instructions in the expander element.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100